(12) UK Patent Application (19) GB (11) 2 264 022 (13) A

(43) Date of A publication 11.08.1993

(21) Application No 9301681.4

(22) Date of filing 28.01.1993

(30) Priority data
(31) 04038534 (32) 29.01.1992 (33) JP
04196055 30.06.1992

(71) Applicant
Fuji Xerox Co. Ltd

(Incorporated in Japan)

No. 3-5 Akasaka 3-chome, Minato-ku, Tokyo, Japan

(72) Inventors
Kazuhiko Mikami
Jun Yamashita
Kazuhiro Suzuki

(74) Agent and/or Address for Service
Marks & Clerk
Alpha Tower, Suffolk Street, Queensway, Birmingham, B1 1TT, United Kingdom

(51) INT CL[5]
H04N 1/21 1/32

(52) UK CL (Edition L)
H4F FDB FS25L FS25R FS30K FS41
U1S S2242

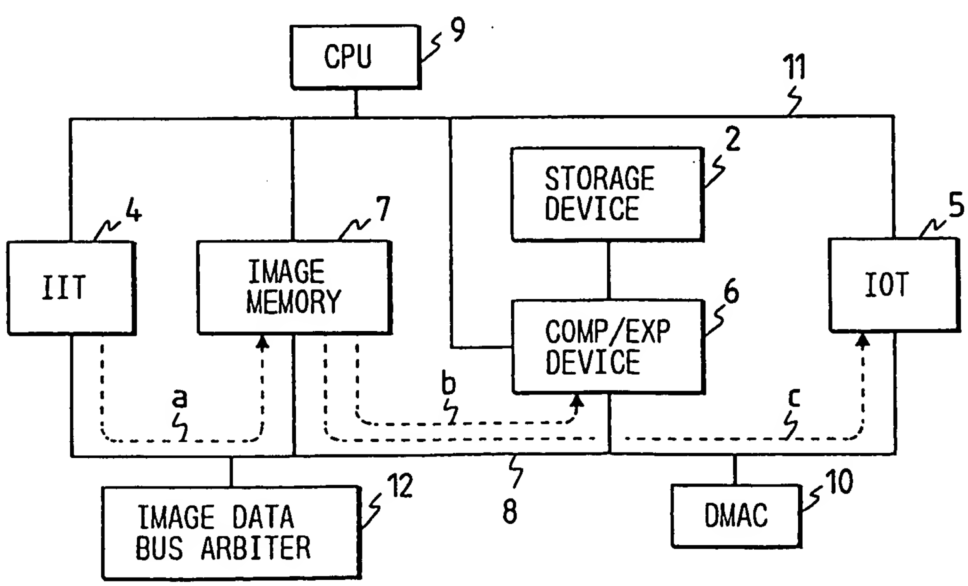
(56) Documents cited
US 5124798 A US 4748513 A

(58) Field of search
UK CL (Edition L) H4F FDB, H4P PPNB
INT CL[5] H04N 1/21 1/32
Online databases: WPI

(54) **Data bus control of image reproducer**

(57) The image reproducer has an image scanner (4), an image output device (5) and a storage device (2), all connected to an image data bus (8). A bus arbiter (12) controls the flow of data along the data bus (8) such that the operation of storing and outputting the image data is performed in parallel by time division control (a, b, c). For the production of n copies of n pages, the first copy is input, output and stored simultaneously, with further copies being read from the storage device (2). The bus arbiter (12) further allows the use of data bus to be prioritised, giving the image scanner (4) and image output device (5) (which operate at a predetermined speed) a higher priority than the compression/expansion device (6) associated with the storage device (2) (which operates at an undefined speed). This reduces the time in which the data bus is vacant and therefore improves its efficiency.

FIG. 6



At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

GB 2 264 022 A

FIG. 1

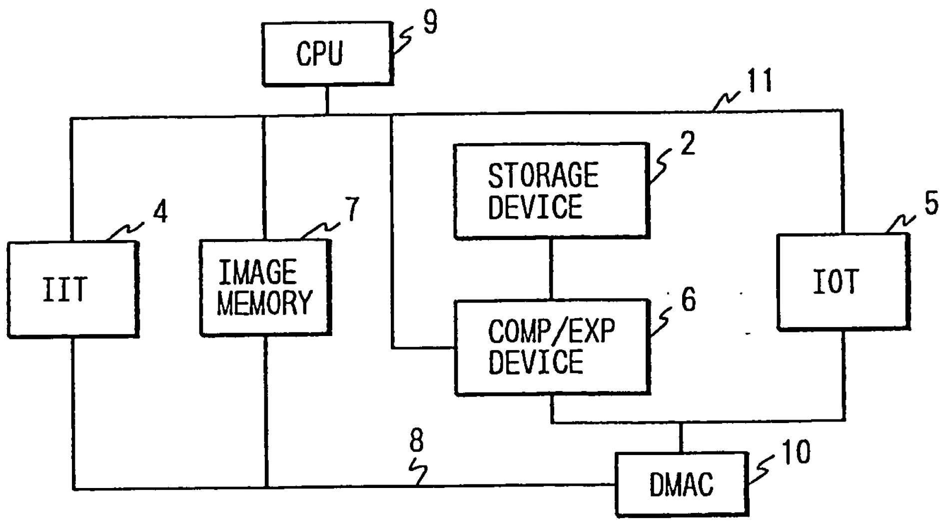

CPU
9
11
STORAGE DEVICE
2
4
7
5
IIT
IMAGE MEMORY
IOT
6
COMP/EXP DEVICE
8
10
DMAC

FIG. 2

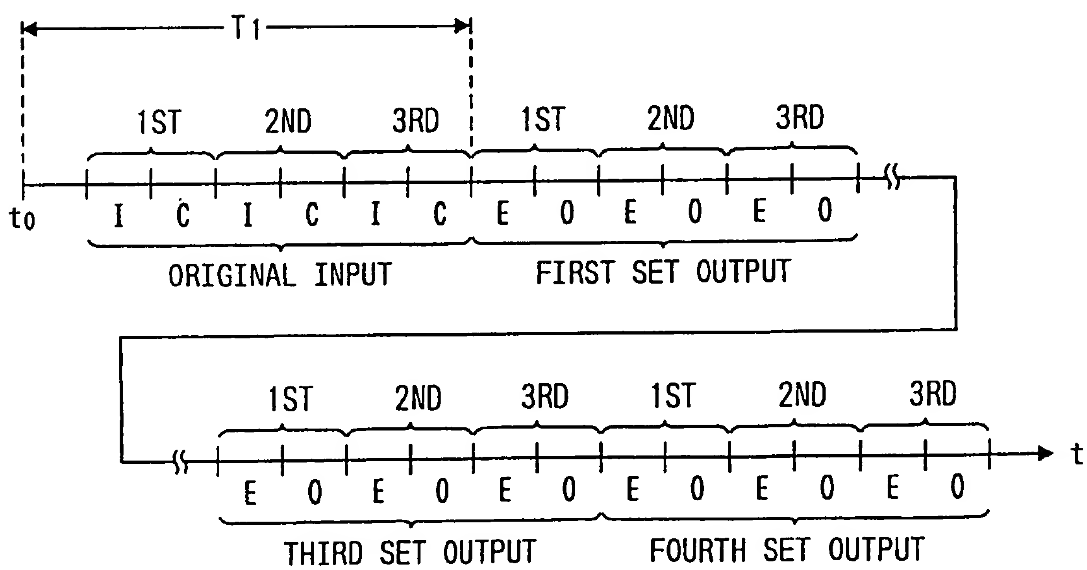

T1
1ST
2ND
3RD
1ST
2ND
3RD
to
I C I C I C E 0 E 0 E 0
ORIGINAL INPUT
FIRST SET OUTPUT
1ST
2ND
3RD
1ST
2ND
3RD
t
E 0 E 0 E 0 E 0 E 0 E 0
THIRD SET OUTPUT
FOURTH SET OUTPUT

FIG. 3

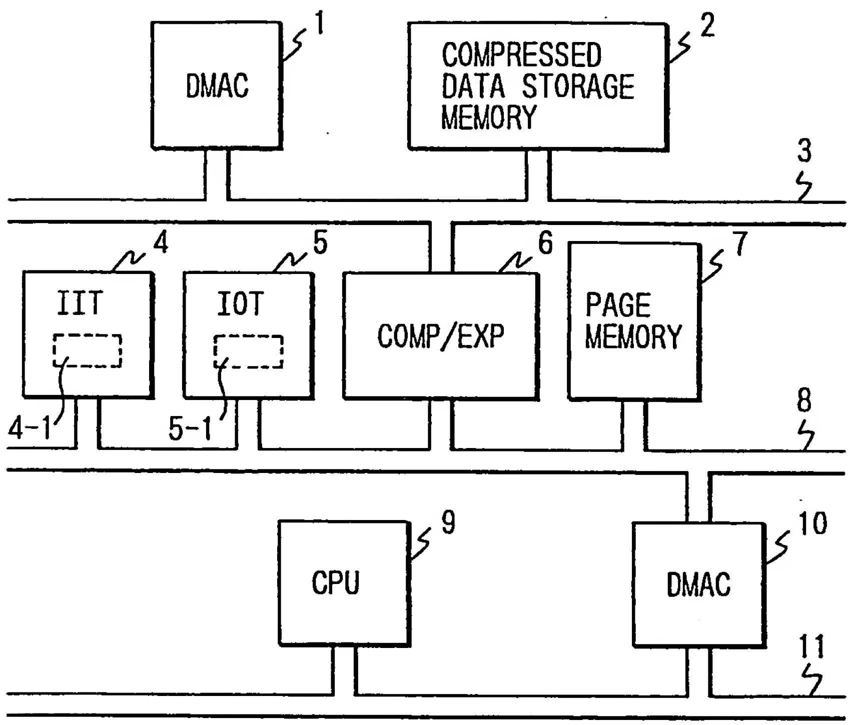
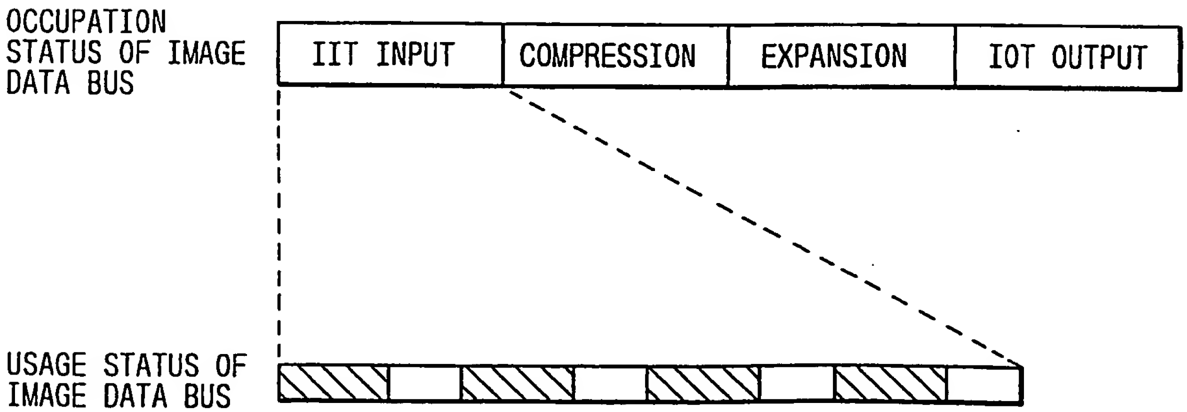

DMAC
1
COMPRESSED DATA STORAGE MEMORY
2
3
IIT
4
IOT
5
COMP/EXP
6
PAGE MEMORY
7
4-1
5-1
8
CPU
9
DMAC
10
11

FIG. 4


OCCUPATION STATUS OF IMAGE DATA BUS
IIT INPUT
COMPRESSION
EXPANSION
IOT OUTPUT
USAGE STATUS OF IMAGE DATA BUS

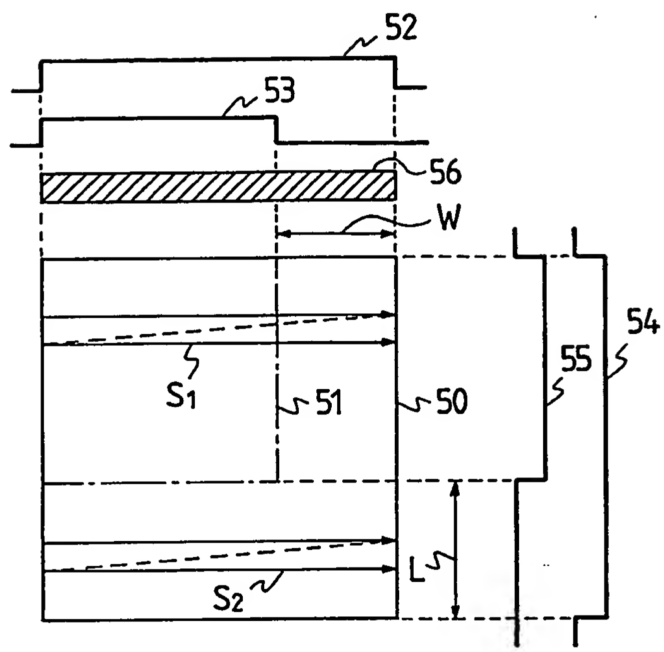

52
53
56
W
54
55
S1
51
50
L
S2

FIG. 5

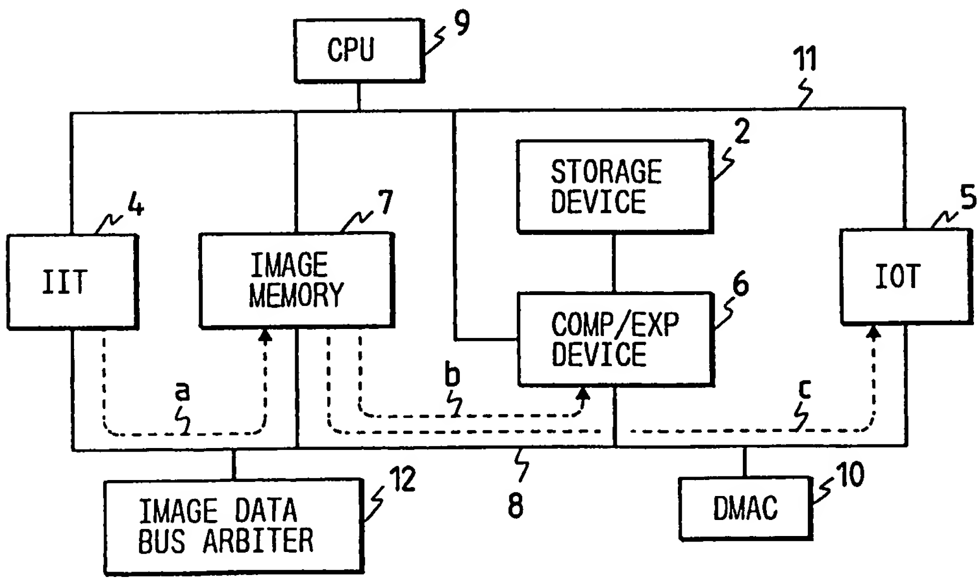

CPU
9
11
STORAGE DEVICE
2
4
IIT
IMAGE MEMORY
7
COMP/EXP DEVICE
6
5
IOT
a
b
c
12
IMAGE DATA BUS ARBITER
8
DMAC
10

FIG. 6

FIG. 7

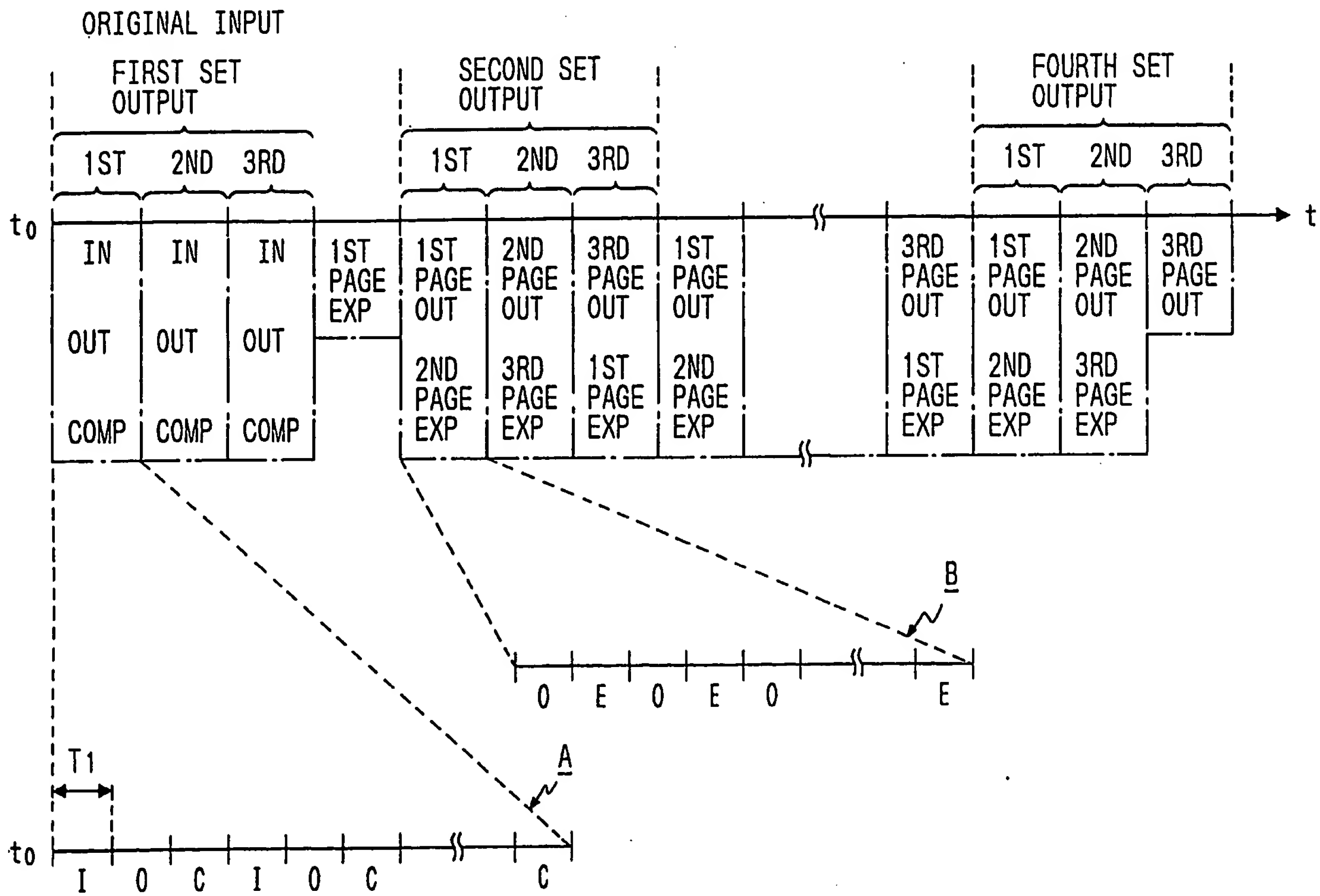

ORIGINAL INPUT
FIRST SET OUTPUT
1ST
2ND
3RD
SECOND SET OUTPUT
FOURTH SET OUTPUT
t0
t
IN
OUT
COMP
1ST PAGE EXP
1ST PAGE OUT
2ND PAGE OUT
3RD PAGE OUT
2ND PAGE EXP
3RD PAGE EXP
1ST PAGE EXP
T1
I O C I O C C
O E O E O E
A
B

FIG. 8

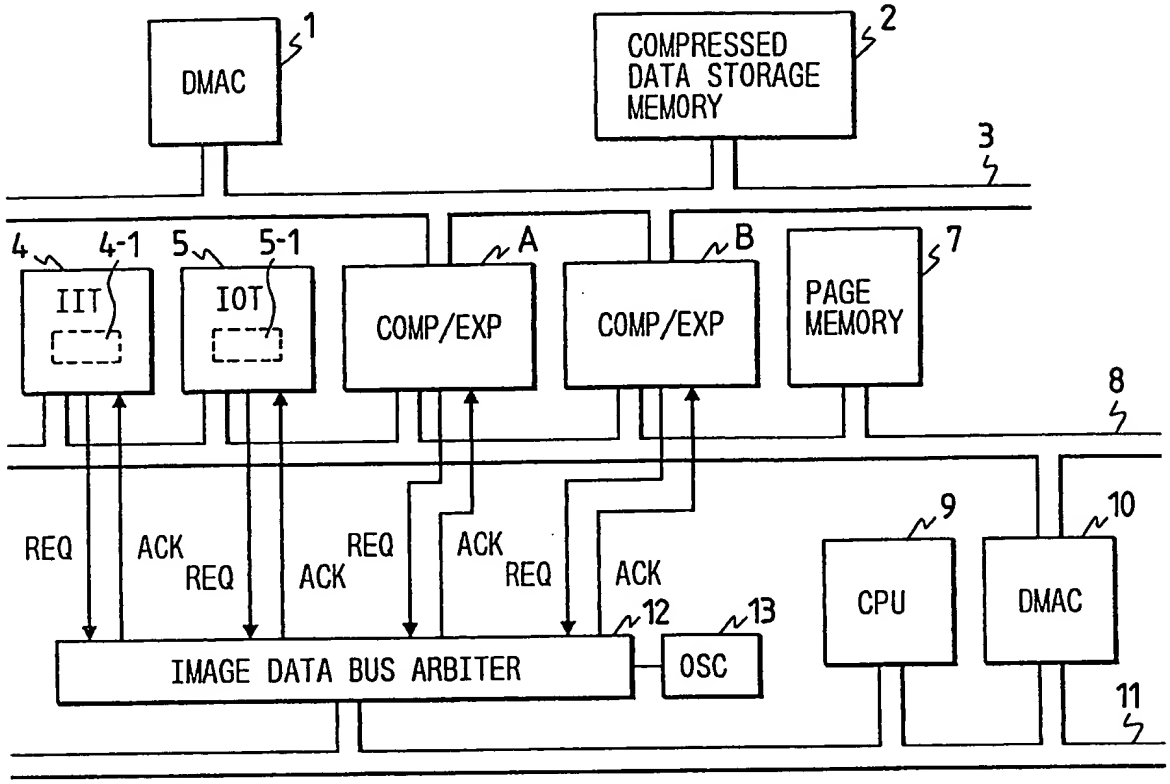

DMAC
1
COMPRESSED DATA STORAGE MEMORY
2
3
4
4-1
IIT
5
5-1
IOT
COMP/EXP
A
COMP/EXP
B
PAGE MEMORY
7
8
REQ
ACK
REQ
ACK
REQ
ACK
REQ
ACK
9
CPU
10
DMAC
12
13
IMAGE DATA BUS ARBITER
OSC
11

FIG. 9

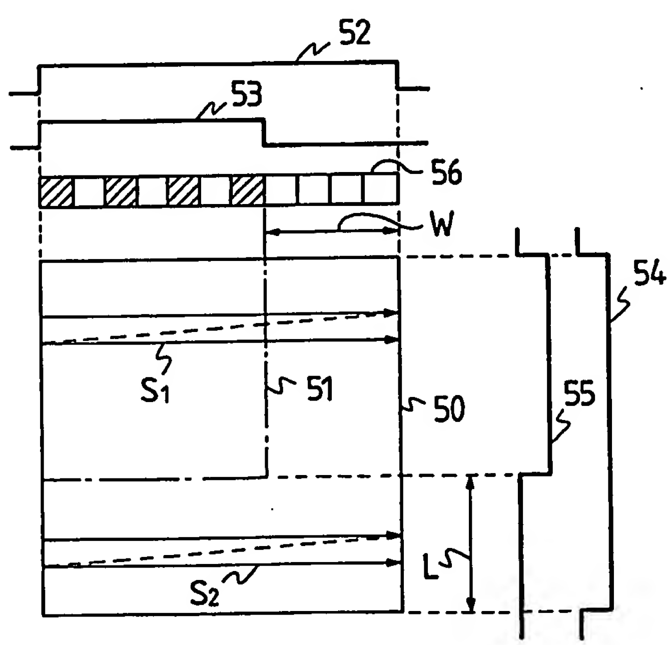

52
53
56
W
54
S1
51
50
55
L
S2

FIG. 10

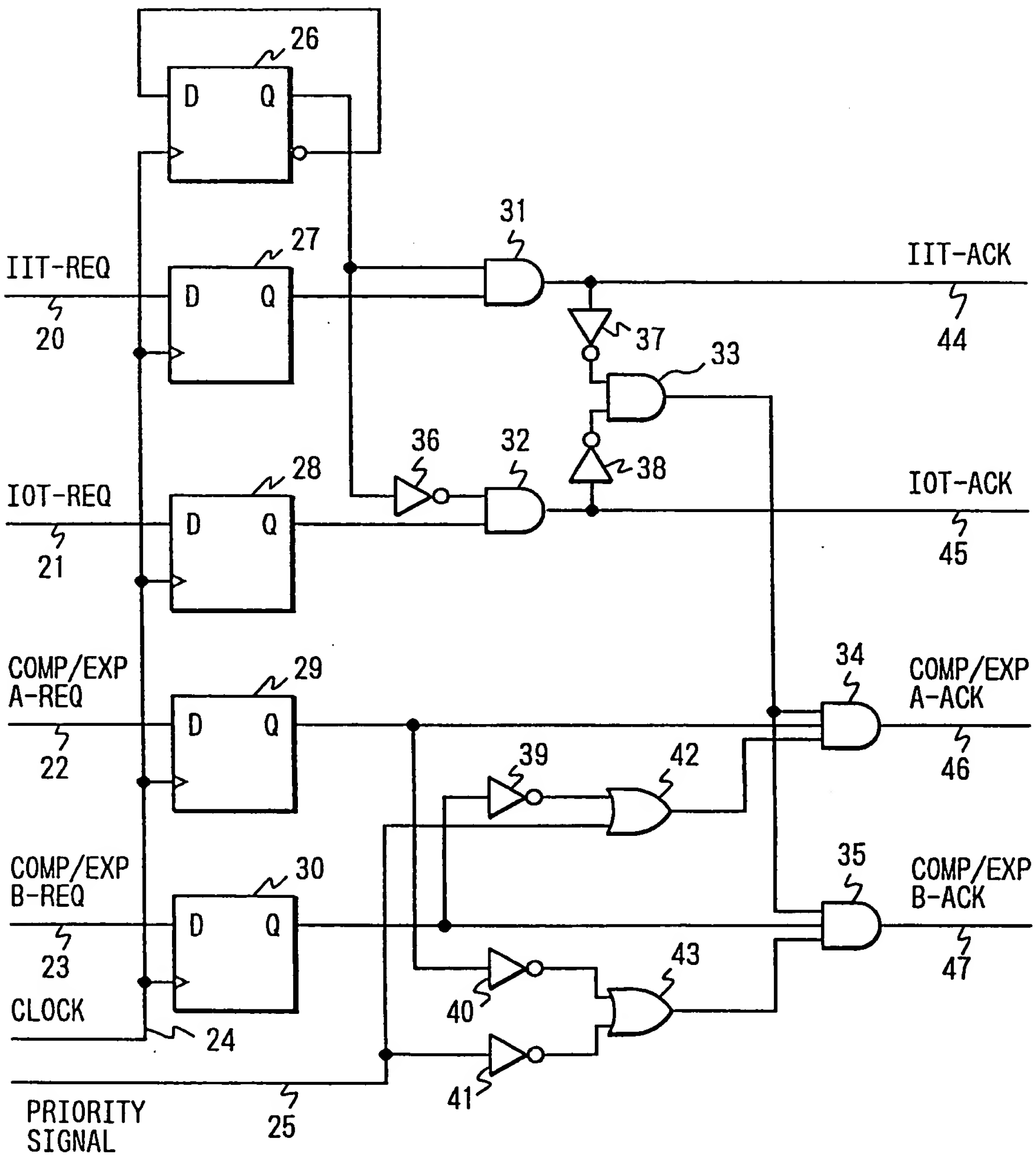

26
D
Q
27
D
Q
IIT-REQ
20
31
IIT-ACK
44
37
33
36
32
28
IOT-REQ
D
Q
21
38
IOT-ACK
45
COMP/EXP
A-REQ
29
D
Q
22
34
COMP/EXP
A-ACK
46
39
42
COMP/EXP
B-REQ
30
D
Q
23
35
COMP/EXP
B-ACK
47
CLOCK
24
40
43
41
PRIORITY
SIGNAL
25

FIG. 11

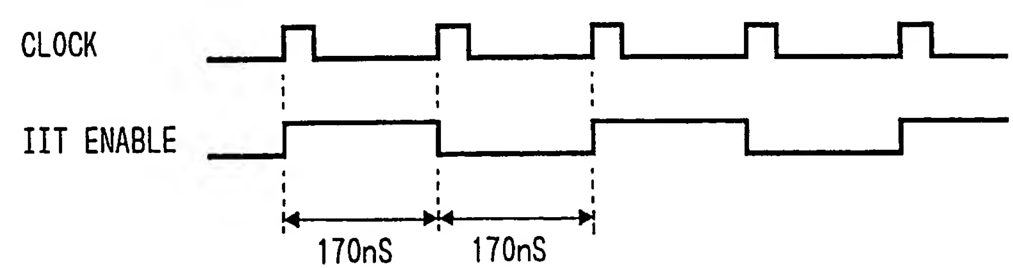
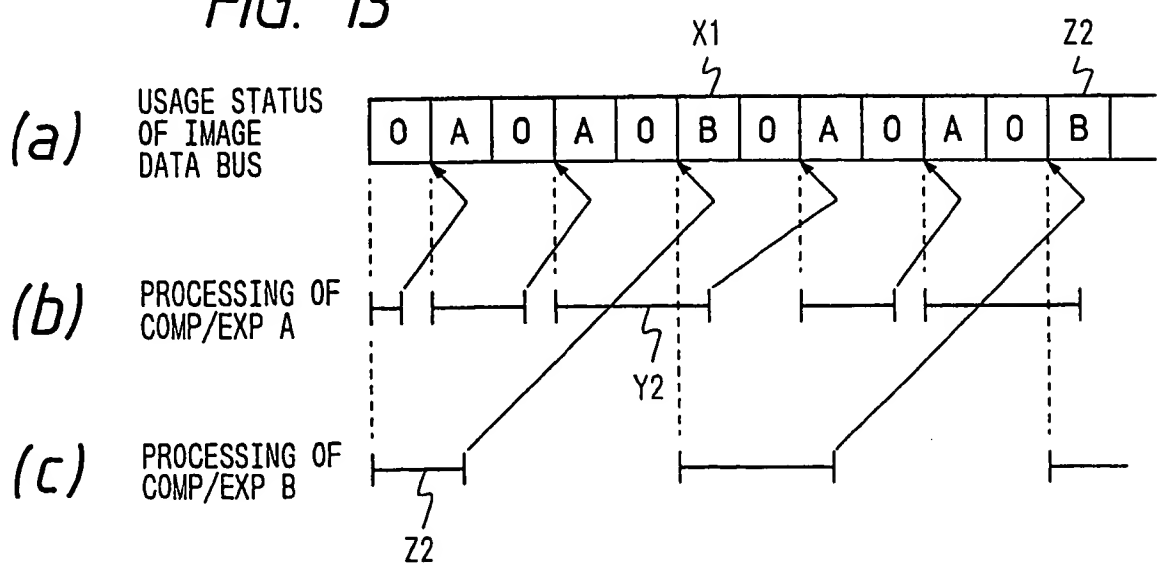
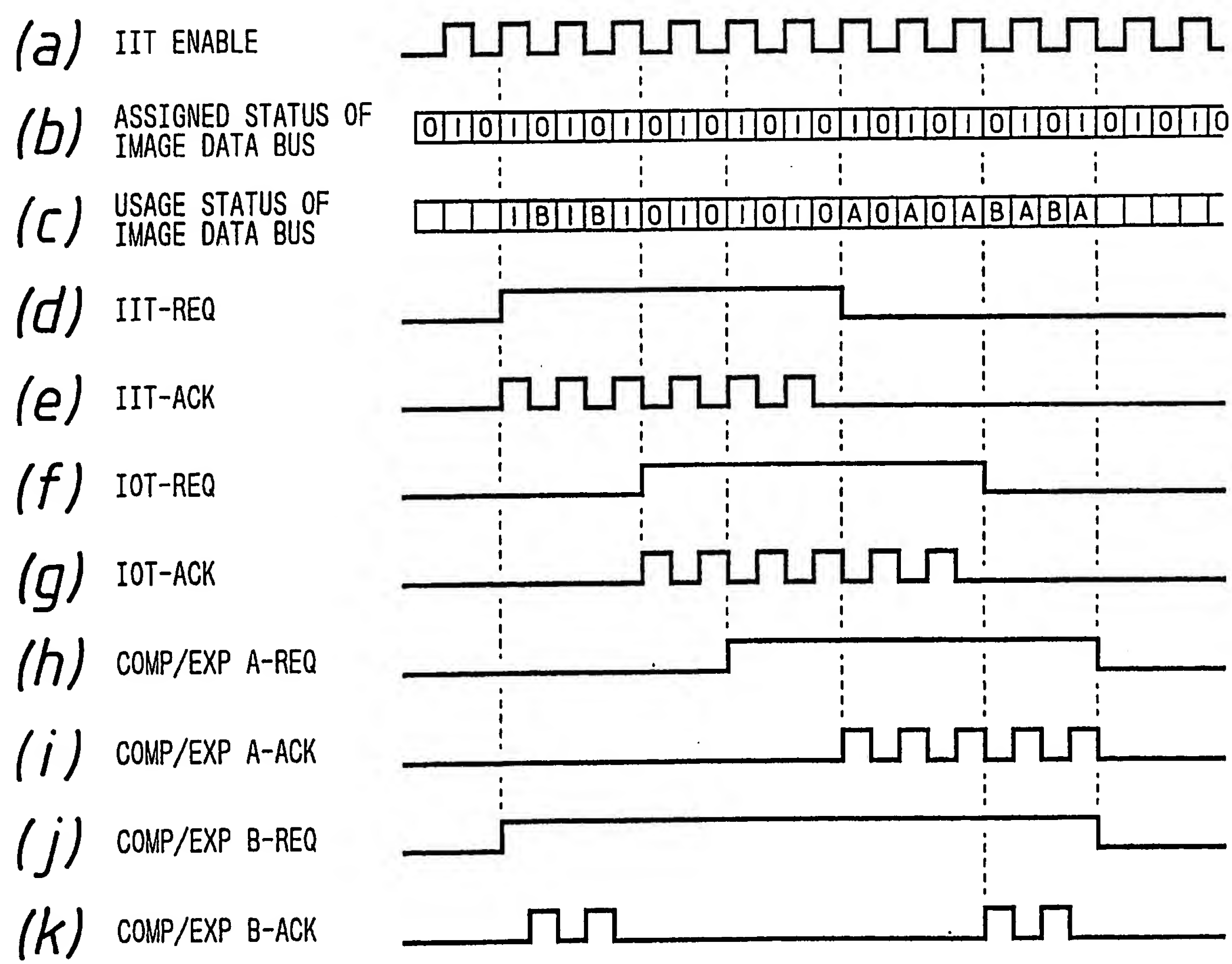

CLOCK
IIT ENABLE
170nS
170nS

FIG. 13


(a)
USAGE STATUS OF IMAGE DATA BUS
(b)
PROCESSING OF COMP/EXP A
(c)
PROCESSING OF COMP/EXP B
X1
Z2
Y2
Z2
0
A
0
A
0
B
0
A
0
A
0
B

8/8

FIG. 12


(a) IIT ENABLE
(b) ASSIGNED STATUS OF IMAGE DATA BUS
(c) USAGE STATUS OF IMAGE DATA BUS
(d) IIT-REQ
(e) IIT-ACK
(f) IOT-REQ
(g) IOT-ACK
(h) COMP/EXP A-REQ
(i) COMP/EXP A-ACK
(j) COMP/EXP B-REQ
(k) COMP/EXP B-ACK

2264022

IMAGE PROCESSING APPARATUS

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to an image processing apparatus in which data transfers between an image input section, an image output section, a compression/expansion device, a page memory and the like are performed via an image data bus.

2. Description of the Conventional Art

In an image processing apparatus such as a digital copying machine, image data which have been obtained by reading an original are first encoded by a compression/expansion device and stored into a storage device. The encoded data is then read out from the storage device by decoding, and printed. In such image processing apparatus, it is possible to decode data of a desired page, and to output a desired number of copies of that page. Namely, such image processing apparatus can electronically perform sorting.

Fig. 1 is a block diagram showing the configuration of such a conventional image processing apparatus. In Fig. 1, the reference numeral 9 designates a central processing unit (CPU), 11 designates a CPU bus, 4 designates original read means (hereinafter, referred to as "IIT (Image Input Terminal)"), 7 designates an image memory, 6 designates compression/expansion device, 2 designates a storage device, 5 designates copy output

means (hereinafter, referred to as "IOT (Image Output Terminal)"), 8 designates an image data bus, and 10 designates a DMAC (Direct Memory Access transfer Controller). The DMAC 10 controls data transfer on the image data bus 8. The data transmission among the IIT, IOT, compression/expansion device, etc. are performed by the DMA (Direct Memory Access)-transfer via an image data bus.

In this image processing apparatus, the IIT 4 consists of an image scanner or the like, and the IOT 5 consists of a printer. The compression/expansion device 6 encodes image data read out from the page memory 7 to compress them, and decodes encoded data read out from the storage device 2 to expand them.

Fig. 2 is a time chart showing the operation of the above-mentioned conventional image processing apparatus. The reference symbol "t" represents time and t_0 indicates an operation start time. In Fig. 4, "I" represents an input operation, "C" represents a compression operation, "E" represents an expansion operation, and "O" represents an output operation. The operation of the apparatus will be briefly described by taking an example where four sets of copies are obtained from an original of three pages.

First, in response to the operation of the operator, the IIT 4 reads the first page of the original. The image data are transferred to the page memory 7. These processes correspond to the input operation. Next, the image data are transferred from the page memory 7 to the compression/expansion device 6

which in turn encodes the data to compress them. The encoded data are stored in the storage device 2. These processes correspond to the compression operation. By the above two operations, the input of image data of the first page of the original is finished. The image data of the second and third pages of the original are input in the same manner. Since the page memory 4 can store image data for only one page of the original, the data of one page of the original are transferred to and compressed in the compression/expansion device 6, and thereafter the input operation for the data of the next page of the original is performed.

After all the pages of the original are read, a first set of copies is started to be output. First, the compressed data for the first page are read out from the storage device 2 and transferred to the compression/expansion device 6 which in turn expands the data. The expanded data are developed in the image memory 4. Then, the data are supplied to the IOT 5 to be output. Thus, the copy of the first page is completed. The copies of the second and the third pages are output in the same manner, respectively. Thus, the copy of the first set is completed. The second, third and forth sets of copies are output in the same manner, respectively.

In the above example, the case where all the three pages of the input original are output as copies has been described. In another case where only a desired page (e.g., only a second

page) is to be output as a copy, only the encoded data for this page is decoded and the copy of this page is output.

Fig. 3 is a block diagram showing the configuration of such a conventional image processing apparatus. In Fig. 3, reference numeral 1 designates a DMAC (Direct Memory Access Controller); 2, a compressed data storing memory; 3, a local DMA bus; 4, an IIT, 4-1 designates a buffer; 5, an IOT; 5-1, a buffer; 6, a compression/expansion device; 7, a page memory; 8, an image data bus; 9, a CPU (Central Processing Unit); 10, a DMAC; and 11 designates a system bus.

When image data are input into the image processing apparatus, the image data are once stored in the buffer 4-1 of the IIT 4. Then, the stored data are DMA-transferred to, for example, the page memory 7 via the image data bus 8 by taking a predetermined amount of the stored data as a unit. When the image data which are developed in the page memory 7 are to be output to a printer or the like, the image data are once DMA-transferred from the page memory 7 to the buffer 5-1 of the IOT 5 via the image data bus 8, and then output. The above transfers are controlled by the DMAC 10. The DMAC 10 is activated by an instruction supplied from the CPU 9 via the system bus 11..

In a case where input image data are required to be first encoded, the input image data are transferred to the compression/expansion device 6. The image data are compressed (or encoded) by the compression/expansion device 6 and then

DMA-transferred to the compressed data storing memory 2. When the compressed data stored in the compressed data storing memory 2 are to be output as image data, the compressed data are expanded by the compression/expansion device 6 and then output. The DMA transfer between the compression/expansion device 6 and the compressed data storing memory 2 is controlled by the DMAC 1.

The main components of the image processing apparatus are connected to the image data bus 8, and data transfers between the components are performed via the image data bus 8. In the conventional image processing apparatus, however, unless the DMA transfer between paired components is completed, it is impossible to perform the DMA-transfer between other paired components. When the DMA transfer from the IIT 4 to the page memory 7 is performed, for example, the next DMA transfer from the page memory 7 to the IOT 5 can be performed only after the previous DMA transfer is completed.

Such a conventional image processing apparatus is disclosed in, for example, Unexamined Japanese Patent Publication (Kokai) Sho-62-176374 and Sho-62-266922.

However, the above-mentioned conventional image processing apparatus has the following problems. The first one is in that the operator remains to be is in anxiety for a long time period from a time when the original is started to be read to a time when the copy is started to be output. The second one is in that the output start time is late so that the total operation

time period is long. Furthermore, the third one is that plural kinds of processes of DMA-transferring image data via the image data bus cannot be performed simultaneously in parallel. This causes that the period during which the image data bus is not used and is vacant is relatively long, thereby impeding the improvement in processing speed.

The first problem is described. In Fig. 2, the output start waiting time period is represented by a time period T_1 from the operation start time t_0 to a time when the copy of the first set is started to be output. The operator must wait during this time period without receiving any response from the image processing apparatus. Therefore, in some cases, the operator worries about whether the copy might be safely output or not, and is in anxiety.

Next, the second problem is described. The total operation time period is a time period from a time when the input of the original is started to a time when the copy of the desired number of sets is completed. However, in the conventional image processing apparatus, the copy of the first set is started after the output start waiting time period T_1 elapses. Accordingly, the total operation time period is constituted by the combination of a time period for the actual copying operation and the output start waiting time period T_1, resulting in that the total operation time period is very long.

Fig. 4 illustrates a use state of the image data bus in the conventional image processing apparatus. Conventionally, a DMA

transfer via the image data bus (e.g., a DMA transfer in the process of inputting image data from the IIT, and a DMA transfer in the compression process) cannot be performed until another DMA transfer is completed. An example of the occupation state of the image data bus is shown in Fig. 4. As seen from the figure, two kinds of processes such as the process of inputting image data from the IIT 4 to the page memory 7 and the process of outputting input image data from the page memory 7 to the IOT 5 cannot be performed simultaneously in parallel.

Moreover, if the image data bus is occupied by one kind of transfer, the image data bus may not be used and may be vacant for a certain time period depending on the image size. This impedes the improvement in processing speed of the image processing apparatus. Fig. 7 is an expanded diagram showing the actual use of the image data bus in a time period when the image data bus is occupied for the "IIT input" process. In the figure, a hatched portion represents a time period when the image data bus is actually used, and a blank portion represents a time period when the image data bus is not used.

Next, the reason why such a non-use time period occurs is described. Fig. 5 illustrates the size of an original and a time period for using the image data bus in the conventional image processing apparatus. In Fig. 5, 50 designates a maximum size, 51 designates the size of the original, 52 and 53 designate line synchronization signals, 54 and 55 designate

page synchronization signals, 56 designates an image data bus occupation time period within one scanning period, S_1 and S_2 designate scan lines, W designates a remainder width, and L designates a remainder length.

The maximum size 50 is the maximum size of an original which can be processed by the image processing apparatus, and is determined depending on the specification of the apparatus. The original size 51 is the size of the original which is currently input. Therefore, the original size 51 sometimes coincides with the maximum size 50, but in many cases the original size 51 is smaller than the maximum size 50. The remainder width W is the difference in length between the original size 51 and the maximum size 50 in the lateral direction (in a direction along the scan lines). The remainder length L is the difference in length between the original size 51 and the maximum size 50 in the longitudinal direction (in a direction perpendicular to the scan lines).

The scanning in the image input process is performed for the maximum size 50, irrespective of the actual size of the original. Therefore, in a case of the original having the size 51, even though no original to be read exists in an area of the remainder width W and an area of the remainder length L, the scanning is also performed for these areas.

In the conventional image processing apparatus, when an image is input from the IIT 4, the image data bus 8 is occupied for the image input process over one scanning period. In other

words, both when the original is scanned along the scan line S_1 and when an area where the original does not exist is scanned along the scan line S_2, the image data bus 8 is always occupied for the image input process as shown by the image data bus occupation time period 56 (a hatched portion represents the occupation time period).

Although the image data bus 8 is occupied for the image input process over the scanning period, the image data bus 8 is not used during the scanning for the area of the remainder width W and during the scanning for the area of the remainder length L. As shown in Fig. 7, therefore, the image data bus 8 is actually used only in part of the occupied time period, resulting in a poor use efficiency of the image data bus 8. Therefore, the above-mentioned problems occur, thereby impeding the improvement in processing speed.

SUMMARY OF THE INVENTION

An object of the present invention is to solve the above-mentioned problems.

In order to solve the above problems, an image processing apparatus of the present invention comprises: original read means; an image memory for storing image data; copy output means for performing printing operation based on image data transferred from said image memory; a compression/expansion device for performing conversion between image data and encoded data; and a storage device for storing said encoded data, and

further comprises a bus arbiter which controls operation of converting image data to encoded data and operation of printing a first set of copies in such a manner that these two operations are performed by a time division manner in parallel with operation of reading an original.

Furthermore, according to one aspect of the invention, in an image processing apparatus in which image data are DMA-transferred via an image data bus, the apparatus comprises an image data bus arbiter by which the use right of the image data bus is divided into predetermined short time units, the image data bus arbiter assigns the time units to a first device group which is a group of image data bus request devices operating at a predetermined speed, and, only when the first device group does not use the image data bus, the image data bus arbiter assigns the time units to a second device group which is a group of image data bus request devices operating at an undefined speed.

Moreover, according to another aspect of the invention, in an image processing apparatus comprising: an image input section; an image output section; a page memory; a compression/expansion device, image data being DMA-transferred via an image data bus among the sections and device; a first DMA controller for controlling the DMA transfer; a central processing unit; a compressed data storing memory for storing data compressed by the compression/expansion device; and a second DMA controller for controlling a DMA transfer between the compression/expansion device and the compressed data storing memory, the

image processing apparatus further comprises an image data bus arbiter which assigns in an alternate manner the use right of the image data bus to the image input section and the image output section in the unit of a predetermined short time period, and, only when the image input section and the image output section do not use the image data bus, assigns the use right of the image data bus to the compression/expansion device.

When the image processing apparatus comprises a plurality of compression/expansion devices, priorities are given to the compression/expansion devices. Alternatively, the priorities may be arbitrarily changed.

During the operation of inputting an original, (1) the conversion from image data to encoded data by the compression/ expansion device and (2) the copy of the first set by transferring the image data to the copy output means are simultaneously performed in parallel in the time division manner. Thus, the copy of the first set is output in parallel with the read of the original, so that the output start waiting time period can be extremely shortened. Therefore, the operator is free from the anxiety which is likely to be felt by the operator until the copy of the first set is safely output. Moreover, since the copy of the first set is output substantially in parallel with the input of the original, the total operation time period for copying can be shortened.

In the image processing apparatus according to one aspect of the invention, a time period is divided into short assigned unit time periods. The image data bus is used in accordance with the priorities by taking the assigned unit time periods as units. Accordingly, request signals can be accepted at any time from the IIT, the IOT, the compression/expansion device and the like. Furthermore, plural kinds of processes of DMA-transferring image data via the image data bus can be performed simultaneously in parallel.

Moreover, the image data bus is used in a time division manner by taking the assigned unit time periods as units, for the plural kinds of processes which are performed simultaneously in parallel. Accordingly, a time period when the image data bus is not used and is vacant becomes short and the use efficiency is improved. As a result, the total processing time period can be shortened.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram showing the configuration of a conventional image processing apparatus;

Fig. 2 is a time chart illustrating the operation of the conventional image processing apparatus;

Fig. 3 is a block diagram showing the configuration of a conventional image processing apparatus;

Fig. 4 is a diagram illustrating a use state of an image data bus in the conventional image processing apparatus;

Fig. 5 is a diagram illustrating the size of an original and an image data bus use time period in the conventional image processing apparatus;

Fig. 6 is a block diagram showing the configuration of an image processing apparatus according to the present invention;

Fig. 7 is a time chart illustrating the operation of the image processing apparatus according to the present invention;

Fig. 8 is a block diagram showing the configuration of an image processing apparatus of the invention;

Fig. 9 is a diagram illustrating the size of an original and an image data bus use time period in the image processing apparatus of the invention;

Fig. 10 is a diagram showing the configuration of an image data bus arbiter;

Fig. 11 shows waveforms of a clock signal and an IIT enable signal;

Fig. 12 is a time chart illustrating the operation of the image data bus arbiter; and

Fig. 13 is a diagram illustrating a use state of an image data bus in a case where two compression/expansion devices are provided.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Hereinafter, an embodiment of the present invention will be described in detail with reference to the drawings. Fig. 6 is a block diagram showing the configuration of an image

processing apparatus according to the present invention. The reference numerals therein correspond to those in Fig. 1, and the reference numeral 12 designates a bus arbiter. The bus arbiter 12 is provided for controlling the image data bus 8 to be used in a time division manner. In this invention, the occupying time period of the image data bus 8 is divided into short time periods by the bus arbiter 12. The divided time periods are appropriately assigned to "input operation", "output operation", "compression operation", "expansion operation" and the like. As a result, a plurality of process operations are substantially simultaneously performed in parallel, whereby the required time period can be shortened. In Fig. 6, paths a, b and c shown by broken lines represent some of data transfer paths. Next, the operation is described with reference to a time chart.

Fig. 7 is a time chart showing the operation of the image processing apparatus according to the present invention. The reference numerals therein correspond to those in Fig. 2. The symbol A indicates an expanded time chart of the process time period for the first page in the time period of "the original input and the output of the first set". The symbol B indicates an expanded time chart of the process time period for outputting the first page in the time period of "the output of the second set". Also, in this example, the original has three pages and four sets of copies of the original are to be obtained.

The operation for the first page in which the input of the original is started at time t_0 is described with reference to the expanded time chart A. During the first one of the divided time periods (T_1 in Fig. 7), the "input operation" is performed. That is, during this time period, the bus arbiter 12 controls the image data bus 8 to be used for transferring the image data read by the IIT 4 to the image memory 7 (the transfer through the path indicated by broken line a in Fig. 6). Since each of the divided time periods is short, only a part of the original is read during this time period.

During the next one of the divided time periods, the "output operation" is performed. The image data bus 8 is used for transferring the image data which have been input into the image memory 7, to the IOT 5 (the transfer through the path indicated by broken line c in Fig. 6). The printing based on the transferred image data is started. This is the start of the copy of the first set. Therefore, the time period during which the operator must wait from the start of the original input to the start of the first printing (i.e., the output start waiting time period) requires only the short divided time period T_1 (however, a certain time period is consumed for the mechanical parts to start to work, so that the actual time period is somewhat longer). For example, the divided time period T_1 may be set to be 170 nanoseconds, so that the operator feels that the output starts simultaneously with the

input. Therefore, the anxiety felt by the operator when the output start waiting time period is long can be eliminated.

During the next one of the divided time periods, the "compression operation" is performed. Specifically, the image data which have been input in the image memory 7 are transferred to the compression/expansion device 6 (the transfer through the path indicated by broken line b in Fig. 6). In the compression/expansion device 6, the data are encoded to be compressed. The encoded data are supplied to the storage device 2 to be stored therein.

As described above, the three operations of input, output and compression are performed in the time division manner until the input of the first page of the original is finished. Therefore, the operation of outputting the copy of the first set and the compression operation are substantially simultaneous and parallel with the input operation. For the second and third pages of the original, the three operations are performed in the same way.

After the input of the original is completed, the output of the copy of the second, third and fourth sets is started in the following manner. First, the encoded data for the first page of the original which are stored in the storage device 2 are read out and expanded to the original image data in the compression/expansion device 6. The image data are developed in the image memory 7. During this time period, only the expansion operation is performed, and the operation of

outputting image data to the IOT 5 is not performed in parallel. The reason of the above is that, if the output from the image memory 7 to the IOT 5 is performed in parallel and in the time division manner, the image memory 7 may become empty in the middle of this operation so that the data to be output to the IOT 5 is interrupted. The reason will be described more specifically. The expansion speed varies depending on the complexity of the image, and hence the speed at which the expanded data are stored into the image memory 4 is not constant. If the data are output from the image memory 4 to the IOT 5 at a constant speed, therefore, the data to be output may be interrupted.

The output of the first page of the second set is started after the expansion of the data for the first page is finished. During this time period, the operation of expanding the data for the second page is performed in parallel in the time division manner. These operations will be described with reference to the expanded time chart B. During one of the divided time periods, portions of expanded data related to the first page are transferred from the image memory 7 to the IOT 5 (the transfer through the path indicated by broken line c in Fig. 6), and a part of the first page of the original is output. During the next one of the divided time periods, the encoded data for the second page is expanded. The expanded data are transferred from the compression/expansion device 6 to the image memory 7 (the reverse transfer through the path

indicated by broken line <u>b</u> in Fig. 6). This process is repeated until the output of the first page and the expansion of the data for the second page are completed.

The output of the second and third pages of the second set is performed in the same way. While the page under the output operation is shifted by one page from the page under the expansion operation, the output operation and the expansion operation are sequentially performed in parallel, so as to output the third and fourth sets. Therefore, during the last one of the divided time periods, as illustrated, only the operation of outputting the third page, i.e., the last page of the fourth set is performed.

As described above, the first copy set is output during the input of the original. After the completion of the input operation, therefore, only the remaining sets are output. Accordingly, as compared with the conventional image processing apparatus in which all the copy sets are output after the completion of the input operation, the total operation time period can be shortened.

Another reason why the total operation time period is shortened is that the image data bus 8 is effectively used in the time division manner. In the conventional image processing apparatus, even when the image data bus 8 is assigned for an operation, for example, the compression operation, data do not always flow through the bus during the assigned time period or the bus may sometimes be vacant. By contrast, in the image

processing apparatus of the present invention, the operation time period is divided into short time periods and the divided time periods are assigned to different operations. Therefore, the vacant time period of the bus line does not continue for a long time period, and the process rapidly advances. As a result, the total operation time period is shortened.

Hereinafter, another embodiment of the invention will be described in detail with reference to the drawings. Fig. 8 shows a block diagram showing the configuration of an image processing apparatus of the invention. The reference numerals in Fig. 8 correspond to those in Fig. 3, and A and B designate compression/expansion devices, 12 designates an image data bus arbiter, and 13 designates an oscillator. The configuration of the image processing apparatus of the invention differs from that of the conventional apparatus in that the image data bus arbiter 12 and the oscillator 13 are provided. The image data bus arbiter 12 adjusts the assigned time periods for using the image data bus 8. The oscillator 13 generates a clock signal. Alternatively, the clock signal may be generated using a clock generator (not shown) which is inherently included in the image processing apparatus.

Fig. 8 shows the embodiment which comprises two compression/expansion devices. In the embodiment, a single image is divided into two parts, and the divided parts are respectively processed by the compression/expression devices in parallel. Thus, the processing speed is improved. It is

obvious to those skilled in the art that this invention may be applied also to an apparatus which comprises only one compression/expansion device.

In this invention, a time period is divided into predetermined short time periods, i.e., assigned unit time periods. The use right of the image data bus 8 is assigned by taking the assigned unit time periods as units. The assignment is performed on the following bases.

(1) Assignment of highest priority: The use right is assigned in an alternate manner to the IIT and the IOT which operate at a predetermined speed.

(2) Assignment of second highest priority: When the IIT and the IOT do not utilize the assigned time periods, the assigned time periods are assigned to the compression/expansion device. In a case where a plurality of compression/expansion devices are provided, priorities are given to the plurality of compression/expansion devices, respectively. The assignment is performed in accordance with the priorities.

(3) Use permission which is given only when it is requested: In any case, when the image data bus is to be actually used by a component, the component should send a request signal (REQ) for using the image data bus and receive an acknowledge signal (ACK).

The highest priority for the assignment is given to the IIT 4 and the IOT 5, because they are designed to operate at a predetermined speed and hence there exists a speed restriction

that the DMA transfer must be performed at the predetermined speed. That is, the operation speed of the IIT 4 and the IOT 5 is determined by mechanical design conditions and is constant.

When the IIT 4 operates, for example, image data are input continuously at a predetermined speed corresponding to the operation speed of an image read mechanism such as an image scanner. The image data are once stored in the buffer 4-1, but the buffer 4-1 cannot store data of an amount greater than a predetermined capacity. Therefore, before the amount of data stored in the buffer 4-1 reaches the predetermined capacity, the stored data must be transferred to a destination (e.g., to the page memory 7). Accordingly, it is necessary to assign the use right of the image data bus 8 with the highest priority.

On the other hand, unlike the IIT 4 and the IOT 5, the compression/expansion devices A and B have no speed restriction. Accordingly, the compression process or the expansion process can be stopped or restarted at any time. Therefore, the DMA transfer related to the compression/expansion devices A and B can be performed after the image data bus 8 becomes vacant. As a result, the second highest priority for assigning the image data bus 8 is given to the compression/expansion devices A and B. In the case shown in Fig. 1 where a plurality of compression/expansion devices are provided, priorities are given to the compression/expansion devices (for example, in the order of A and B).

Fig. 9 illustrates the size of an original and a time period for using the image data bus in the image processing apparatus of this invention. The reference numerals in Fig. 9 correspond to those in Fig. 5. Fig. 9 shows an example where the original having the size 51 is read by the image scanner and the image data are input via the IIT 4.

Fig. 9 is different from Fig. 5 in a portion corresponding to the image data bus occupation time period 56. The portion indicates the scanning along the scan line S_1 which traverses the original. A time period is divided into predetermined short time periods, i.e., assigned unit time periods. The assigned unit time periods are alternately assigned to the IIT 4 and the IOT 5. The IIT 4 occupies the image data bus 8 only in the assigned unit time periods during which the line synchronization signal 53 is produced among the assigned unit time periods which are assigned to the IIT 4 (hatched portions represent occupation time periods).

When the scanning proceeds and the scanning along the scan line S_2 lower than the lower end of the original having the size 51 is to be performed, the line synchronization signal 53 becomes 0. As a result, the IIT 4 is not allowed to occupy the image data bus 8. Even in the time periods for scanning, in the assigned unit time periods for scanning the area of the remainder width W or the area of the remainder length L (i.e., in the time periods when the IIT 4 does not substantially operate) among the assigned unit time periods which are

assigned to the IIT 4, the IIT 4 devolves the use right of the image data bus 8 upon the compression/expansion device A or B.

As a result, the use efficiency of the image data bus 8 is enhanced, and the processing speed can be improved. Moreover, a plurality of kinds of DMA transfers can be performed simultaneously in parallel, whereby the processes of image input, compression, expansion, image output and the like can be performed simultaneously in parallel.

(Configuration of the image data bus arbiter)

The image data bus arbiter 12 is provided for assigning the use right of the image data bus 8 on the above-mentioned bases and for allowing the components to use the image data bus 8. Fig. 10 specifically shows the configuration of the image data bus arbiter 12. In Fig. 10, 20-25 designate signal lines, 26-30 designate D flip-flops, 31-35 designate AND circuits, 36-41 designate inverters, 42 and 43 designate OR circuits, and 44-47 designate signal lines.

A clock signal from the oscillator 13 in Fig. 8 is supplied to the signal line 24, and then given to the clock inputs of the D flip-flops 26-30. The D flip-flop 26 produces an IIT enable signal from the output Q based on the clock signal. Fig. 11 shows waveforms of the clock signal and the IIT enable signal. The IIT enable signal has a rectangular waveform with the half period which is equal to the period of the clock signal (e.g., 170 nanoseconds).

The D flip-flops 27-30 receive request signals from the IIT 4 and the like for requesting the use of the image data bus 8, and output the signals in synchronization with the clock signal. To the D flip-flop 27, the request signal from the IIT 4 is input, and, to the D flip-flop 28, the request signal from the IOT 5 is input.

The outputs from the flip-flops 27 and 28 are coupled to respective inputs of the two-input AND circuits 31 and 32. The IIT enable signal is supplied to the other input of the AND circuit 31. A signal which is obtained by inverting the IIT enable signal in the invertor 36 is supplied to the other input of the AND circuit 32.

Accordingly, the gates of the AND circuits 31 and 32 are alternately enabled in accordance with the IIT enable signal. During the gate enable period, if the output from the D flip-flop 26 or 27 is supplied to the AND circuit 31 or 32, it is output via the signal line 44 or 45 as an acknowledge signal.

The D flip-flops 29 and 30 respectively output the request signals from the compression/expansion devices A and B in synchronization with the clock signal. These signals are supplied to respective inputs of the three-input AND circuits 34 and 35. To another one of the three inputs, the output of the two-input AND circuit 33 is coupled. The two inputs of the AND circuit 33 are coupled to the outputs of the AND circuits 31 and 32 via the inverters 37 and 38, respectively.

Therefore, the AND circuit 33 outputs a signal of high level only when the acknowledge signals to the IIT 4 and the IOT 5 are not output. As a result, the acknowledge signals to the IIT 4 and the IOT 5 are allowed to be output with priority to the acknowledge signals to the compression/expansion devices A and B (the first priority).

The priorities of the compression/expansion devices A and B are determined by a priority signal which is input via the signal line 25. When the priority signal is at a high level, the compression/expansion device A has the higher priority. When the priority signal is at a low level, the compression/expansion device B has the higher priority. More specifically, when the priority signal is at the high level, a signal of high level is output from the OR circuit 42. The high-level signal is supplied to the third input of the AND circuit 34, so that the AND circuit 34 becomes into the gate-enable state. At this time, if the request signal from the compression/expansion device A is output from the D flip-flop 29, the request signal is allowed to pass through the AND circuit 34 and output as the acknowledge signal to the compression/expansion device A.

On the other hand, the priority signal of the level which has been changed from high to low by the invertor 41 is supplied to one input of the two-input OR circuit 43. When the request signal from the compression/expansion device A is output from the D flip-flop 29, the other input of the OR circuit 43 receives the request signal of the level which has

been changed from high to low by the invertor 40. Therefore, the OR circuit 43 will not output a signal of high level. Therefore, the AND circuit 35 will not become into the gate-enable state. Even if the request signal is output from the compression/expansion device B, the acknowledge signal to the compression/expansion device B will not be produced. Thus, it is ensured that the compression/expansion device A has the higher priority. If it is required that the compression/expansion device B has the higher priority than the compression/expansion device A, the priority signal supplied via the signal line 25 should be at the low level.

(Operation of the image data bus arbiter)

Fig. 12 is a time chart illustrating the operation of the image data bus arbiter. In Fig. 12, the IIT enable signal (a) is shown in conjunction with Fig. 4. A state (b) where the time period is divided into assigned unit time periods based on the IIT enable signal and the use right of the image data bus 8 is assigned in an alternate manner to the IIT 4 and IOT 5 having the highest assigned priority. The assigned unit time period labeled by "I" represents a time period during which the use right is assigned to the IIT 4, and the assigned unit time period labeled by "O" represents a time period during which the use right is assigned to the IOT 5. This assignment is performed by inputting a signal of high level in an alternate manner to one of the two input terminals of the respective AND

circuits 31 and 32 in Fig. 3, in accordance with the IIT enable signal.

Fig. 12(d) shows the request signal from the IIT 4 (the output of the D flip-flop 27 in Fig. 10). The request signal is output in accordance with the line synchronization signal (53 in Fig. 9), when the original is scanned. Fig. 12(e) shows the acknowledge signal to the IIT 4. The acknowledge signal is output only in the assigned unit time periods of Fig. 12(b) which are labeled by "I" within the time period when the request signal of Fig. 12(d) is output (the signal line 44 in Fig. 10). In the assigned unit time period, the IIT 4 actually uses the image data bus 8. This is represented by the assigned unit time period labeled by "I" in Fig. 12(c).

The assigned time period during which the IOT 5 actually uses the image data bus 8 can be obtained in the same way. The assigned time period is a time period labeled by "O" in Fig. 12(c). That is, the acknowledge signal (Fig. 12(g), the signal on the signal line 45 in Fig. 10) to the IOT 5 is output in the assigned unit time period labeled by "O" in Fig. 12(b) within the time period when the request signal from the IOT 5 (Fig. 12(f), the output of the D flip-flop 28 in Fig. 10).

When the request signal for requesting the use of the image data bus 8 is output from the compression/expansion device A or B, since these devices have lower priorities than the IIT 4 and the IOT 5, the use right of the image data bus 8 is assigned to these devices only in the assigned unit time period when the

acknowledge signal to the IIT 4 or the IOT 5 is not output within the time period when the request signal is output.

It is assumed that the compression/expansion device A is provided with a higher priority than that of the compression/expansion device B. This priority is determined by giving the priority signal of "high" to the signal line 25 in Fig. 10. Thus, the acknowledge signal to the compression/expansion device A (Fig. 12(i)) is output only in the assigned unit time period when both the acknowledge signals of Figs. 12(e) and 12(g) are not output within the time period when the request signal from the compression/expansion device A (Fig. 12(h)) is output. The assigned unit time period is a time period labeled by "A" in Fig. 12(c). In the assigned unit time period, the compression/expansion device A can use the image data bus 8.

The acknowledge signal to the compression/expansion device B is output only in the assigned unit time period when the acknowledged signals to the IIT 4 and the IOT 5 and also the compression/expansion device A are not output within the time period when the request signal of Fig. 12(j) is output (Fig. 12(k)). The assigned unit time period is a time period labeled by "B" in Fig. 12(c). In the time period, the compression/expansion device B can use the image data bus 8.

When two compression/expansion devices are provided, there exists a problem in that the process in the compression/expansion device having the lower priority is delayed. Fig. 13 is a diagram showing a use state of the image data bus in the

case where two compression/expansion devices are provided. In this example, the operation of outputting data to the IOT 5 and the processes in the compression/expansion devices A and B are performed in parallel.

In Fig. 13, a use state of the image data bus is shown. One division represents one of the above-mentioned assigned unit time periods. The label "O" in a division indicates that the IOT 5 uses the image data bus, and the labels "A" and "B" indicate that the compression/expansion devices A and B respectively use the image data bus, respectively. A lateral solid line in Fig. 13(b) represents a time period during which the process in the compression/expansion device A is performed and image data sufficient to perform the DMA transfer are obtained. An arrow directed to Fig. 13(a) indicates the assigned unit time period during which the image data obtained by the process are DMA-transferred. After the transfer, the process is restarted. Similarly, Fig. 13(c) shows the process in the compression/expansion device B.

As described above, the compression/expansion device A is assumed to be prior to the compression/expansion device B. After the process in the compression/expansion device A is finished, therefore, the compression/expansion device A uses the image data bus 8 in the assigned unit time period when the IOT 5 does not use the image data bus 8. However, with respect to an assigned unit time period X1, a process Y1 in the compression/expansion device A is not finished before the start

of the assigned unit time period X1, so that the compression/ expansion device A cannot use the image data bus.

In this case, the compression/expansion device B has finished a process Z1 in which image data sufficient for the DMA transfer are obtained, and waits for the assigned unit time period to be free. Thus, the compression/expansion device B is allowed to use the image data bus 8 in the assigned unit time period X1. Also in an assigned unit time period X2, the compression/expansion device B is allowed to use the image data bus 8.

When the compression/expansion device B has always the lower priority than the compression/expansion device A, the time period during which the compression/expansion device B is allowed to use the image data bus 8 is short as described above. Therefore, the process of an image area for the compression/expansion device B lags far behind the process of an image area for the compression/expansion device A.

In order to prevent this delay from occurring, the priorities of the compression/expansion devices may be changed in the middle of the process for a single image. For example, the CPU 9 in Fig. 8 monitors an address counter (not shown) of the DMAC 10 at regular time intervals (e.g., once per 100 milliseconds), to detect a compression/expansion device the process of which is delayed. A higher priority than before is given to the detected compression/expansion device. In order to reverse the priorities, the level of the priority signal

which is supplied via the signal line 25 in Fig. 3 should be inverted.

As described above, according to the image processing apparatus of the present invention, the output of the first set is started at the same time as the input of the original. Therefore, the anxiety which is likely to be felt by the operator until the output of the first set is safely started after the elapse of a long time period can be eliminated. Moreover, the output of the first set is performed at the same time as the operation of inputting the original, so that, for example, in the case where N copy sets are to be obtained, the remaining (N-1) copy sets only have to be output after the completion of the operation of inputting the original. Therefore, as compared with a conventional image processing apparatus in which all the N copy sets are output after the completion of the operation of inputting the original, the total operation time period for the copy can be shortened.

Furthermore, in the image processing apparatus of the invention, the time period is divided into short time periods, i.e., assigned unit time periods. The image data bus 8 is used in accordance with the priorities by taking the assigned unit time periods as units. Thus, request signals can be accepted at any time from the IIT 4, the IOT 5, the compression device A and B and the like. Therefore, a plurality of kinds of processes including the operation of DMA-transferring image

data via the image data bus 8 can be performed simultaneously in parallel.

Moreover, the image data bus 8 is used for the plurality of kinds of processes which are performed simultaneously in parallel by taking the assigned unit time period as units, so that a time period during which the image data bus 8 is not use and is vacant is shortened, whereby the use efficiency is improved, Therefore, the time required for completing the entire process can be shortened.

CLAIMS:

1. An image processing apparatus comprising:

original read means;

an image memory for storing image data;

copy output means for performing printing operation based on image data transferred from said image memory;

a compression/expansion device for performing conversion between image data and encoded data; and

a storage device for storing said encoded data,

wherein said image processing apparatus further comprises a bus arbiter which controls operation of converting image data to encoded data and operation of printing a first set of copies in such a manner that these two operations are performed by a time division manner in parallel with operation of reading an original.

2. An image processing apparatus in which image data are DMA (Direct Memory Access)-transferred via an image data bus, said image processing apparatus comprising:

an image data bus arbiter by which the use right of said image data bus is divided into predetermined short time units, said image data bus arbiter assigns said time units to a first device group which is a group of image data bus request devices operating at a predetermined speed, and, only when said first device group does not use said image data bus, said image data bus arbiter assigns said time units to a second device group

which is a group of image data bus request devices operating at an undefined speed.

3. An image processing apparatus as claimed in claim 2, wherein said image data bus arbiter comprises clock means for generating said short time units.

4. An image processing apparatus as claimed in claim 2, wherein said image data bus arbiter monitors processings of a plurality of compression/expansion devices for performing conversion between image data and encoded data, said image data bus arbiter changes a priority of said compression/expansion devices in response to a result of the monitoring.

5. An image processing apparatus as claimed in claim 2, wherein said short time unit of said image data bus arbiter is the assigned time unit for said first and second device groups.

6. An image processing apparatus as claimed in claim 2, wherein said assigned time unit is a time interval which is overlapped with a request signal.

7. An image processing apparatus comprising:

an image input section;

an image output section;

a page memory;

a compression/expansion device, image data being DMA-transferred via an image data bus among said sections and device;

a first DMA controller for controlling said DMA transfer;

a central processing unit;

a compressed data storing memory for storing data compressed by said compression/expansion device; and

a second DMA controller for controlling a DMA transfer between said compression/expansion device and said compressed data storing memory,

wherein said image processing apparatus further comprises an image data bus arbiter which assigns in an alternate manner the use right of said image data bus to said image input section and said image output section in the unit of a predetermined short time period, and, only when said image input section and said image output section do not use said image data bus, assigns the use right of said image data bus to said compression/expansion device.

8. An image processing apparatus according to claim 7, wherein said image processing apparatus comprises a plurality of compression/expansion devices, and priorities are given to said compression/expansion devices.

9. An image processing apparatus according to claim 7, wherein said image processing apparatus comprises a plurality of compression/expansion devices, and priorities are given to said compression/expansion devices, said priorities being arbitrarily changeable.

Patents Act 1977
Examiner's report to the Comptroller under Section 17 (The Search Report)

Application number

GB 9301681.4

Relevant Technical fields

(i) UK Cl (Edition L) H4F - FDB H4P - PPNB

(ii) Int Cl (Edition 5) H04N - 1/21, 32

Search Examiner

D H JONES

Databases (see over)

(i) UK Patent Office

(ii) ONLINE DATABASES: WPI

Date of Search

4 MAY 1993

Documents considered relevant following a search in respect of claims 1

Category (see over)	Identity of document and relevant passages	Relevant to claim(s)
A	US 5124798 (FUJI) - see whole document	- - -
X	US 4748513 (CANON) - see lines 8-14 column 8	1

Category	Identity of document and relevant passages	Relevant to claim(s)

Categories of documents

X: Document indicating lack of novelty or of inventive step.

Y: Document indicating lack of inventive step if combined with one or more other documents of the same category.

A: Document indicating technological background and/or state of the art.

P: Document published on or after the declared priority date but before the filing date of the present application.

E: Patent document published on or after, but with priority date earlier than, the filing date of the present application.

&: Member of the same patent family, corresponding document.

Databases: The UK Patent Office database comprises classified collections of GB, EP, WO and US patent specifications as outlined periodically in the Official Journal (Patents). The on-line databases considered for search are also listed periodically in the Official Journal (Patents).

Published 1993 at The Patent Office, Concept House, Cardiff Road, Newport, Gwent NP9 1RH. Further copies may be obtained from Sales Branch, Unit 6, Nine Mile Point, Cwmfelinfach, Cross Keys, Newport, NP1 7HZ. Printed by Multiplex techniques ltd, St Mary Cray, Kent.